Claims 19, 21, 23 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent 5,635,847 ("Seidel") in view of U.S. patent 5,483,421 ("Gedney") and further in view of U.S. patent 5,680,936 ("Beers"). Applicants respectfully traverse this rejection in view of the amended claims for the following reasons, each of which is an independent reason that is individually sufficient to justify allowance of the claims:

1) Independent claim 19 recites soldering cache memory devices to the interposer, and soldering the interposer to a substrate. This argument was made in the previous response, but was not addressed because the claim did not specifically recite the word "soldering". None of the cited references disclose or suggest soldering an interposer and cache memory devices in the claimed manner.

Claims 21-26 depend from claim 19 and therefore contain the same limitations not disclosed or suggested by the cited references. Claims 22, 24 and 25 are not currently under consideration, but will be similarly amended for consistent terminology as necessary once the other pending claims have been allowed.

CONCLUSION

For the aforementioned reasons, Applicants maintain that claims 19, 21, 23 and 26 are now in condition for allowance. Applicants further maintain that since generic claim 19 is in condition for allowance, claims 22, 24 and 25 should now be considered by

the Examiner. No fee is believed due with this response. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOLOKOFF, TAYLOR & ZAFMAN, LLP

Date: 3-12-02 John Travis

John Travis
Reg. No. 43,203

12400 Wilshire Blvd
Seventh Floor
Los Angeles, California 90025-1026
(512) 330-0844

APPENDIX A

MARKED-UP COPY OF AMENDED CLAIMS

19. (Amended six times) A method of assembling a multi-chip device comprising:

providing an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of selected ones of the plurality of conductive pads;

[coupling] soldering a plurality of cache memory devices and at least one passive device to the first surface to form a multi-chip subassembly, wherein the at least one passive device is selected from a group consisting of resistors, capacitors, and inductors;

testing said plurality of cache memory devices on said interposer;

[coupling] soldering said interposer to a substrate with the solder balls after said testing if said plurality of cache memory devices pass said testing; and

[coupling] soldering a microprocessor device to the substrate.